An Overview of Logic Built-In Self-Test Fault Coverage Optimization and Power Efficiency

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***Abstract*—As the size of integrated circuits (ICs) continues to decrease in accordance with Moore's Law, the number of transistors—and thereby gate inputs—in these circuits increases exponentially. To ensure the functionality of these rapidly growing complex digital systems once they are fabricated, test procedures must be put in place such that the expected inputs yield the intended outputs. While automated test equipment (ATE) can be traditionally used for this purpose, logic built-in self-test (LBIST) presents a more efficient on-chip alternative. This approach reduces test costs, improves fault coverage, and enables at-speed testing. However, implementing LBIST in large and complicated circuitry introduces challenges, particularly in optimizing fault coverage and minimizing power consumption. Rather than employing exhaustive 2^n test vectors to map every output state, optimal techniques can be used to significantly improve test efficiency and effectiveness of the LBIST IC. This paper explores existing LBIST techniques, identifies their limitations, and presents advanced approaches to improve both fault coverage and power efficiency. Furthermore, comparative analysis will be used to highlight the benefits of various optimization techniques to ultimately streamline semiconductor testing.**

***Index Terms*—LBIST, ATE, IC, testing efficiency, power consumption, circuit optimization.**

I. Introduction

With the continuous advancement of semiconductor technology, modern-day ICs have reached a remarkable level of size and complexity. This phenomenon has been characterized by Moore's Law, where the number of transistors on a chip doubles approximately every two years [1]. This relationship between the number of microprocessor chip transistors and time (in years) is nicely graphed by Cavin *et al.*. in Figure 1.

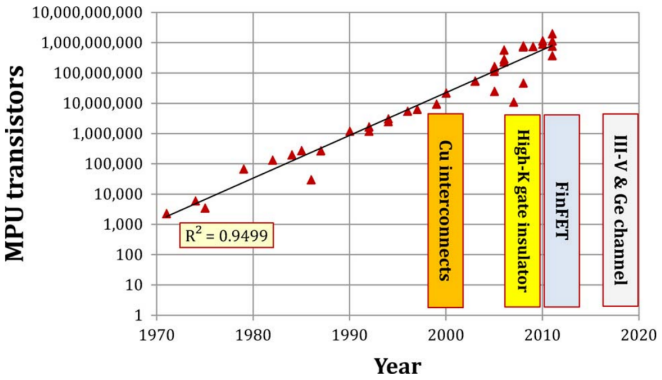

Figure 1: Moore's Law Graphical Relationship between Number of Transistors and Time [1]

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To keep up with this trend, very-large-scale integration (VLSI) design was developed. This process of creating an IC by combining millions or even billions of metal oxide semiconductor (MOS) transistors onto a chip has been widely adopted by the semiconductor industry. For decades, modern technology has focused on continuously shrinking and improving transistor design. While great strides have been made in this regard, new issues began to present themselves. By having such a large number of transistors in circuits, performing fault coverage has proved to be increasingly difficult. Similarly, power consumption has emerged as a critical issue that must always be taken into consideration.

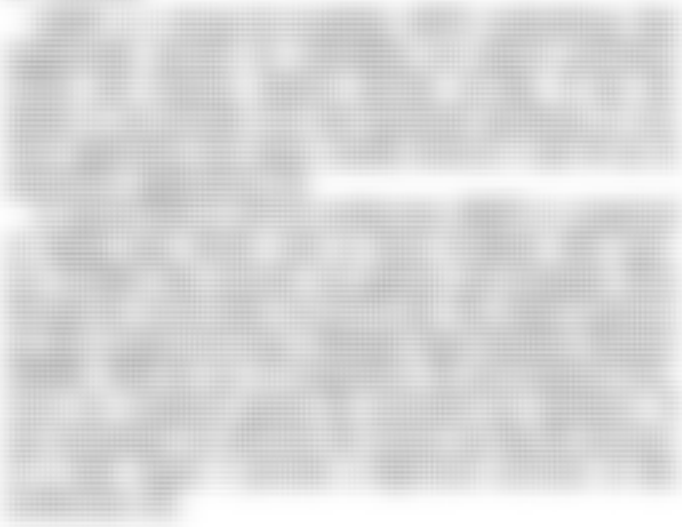
Taking a deeper look into reliability of these ICs, as stated before, modern digital circuits contain potentially billions of transistors. Each can serve a critical purpose in the device operation. If even a single transistor becomes faulty, the system may be heavily impacted. Unintended consequences could occur, ranging from issues such as degraded performance and incorrect computations, to complete system failure.

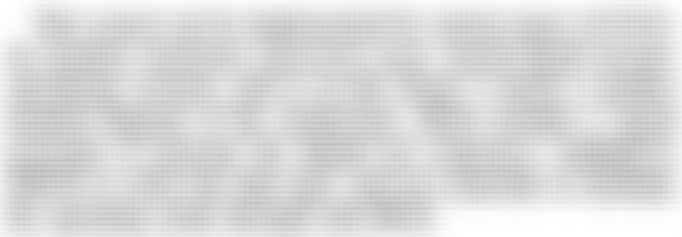
It is thus important to test these large digital circuits to not only detect, but also diagnose manufacturing defects that may pose as a reliability issue in various fields: aerospace, industrial, automotive, and biomedical to name a few. Ensuring correct operation can avoid potentially dangerous incidents.

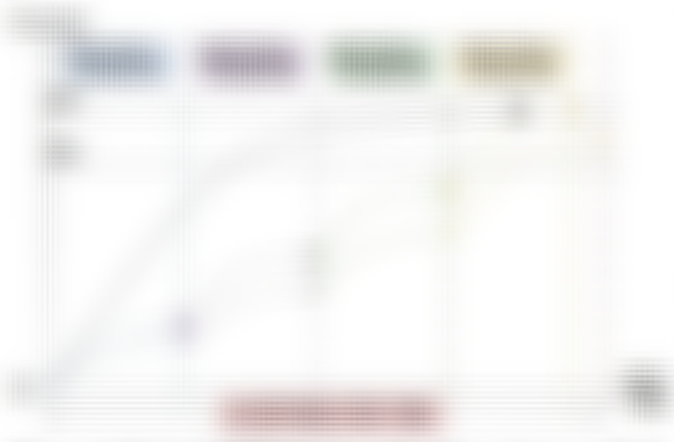
Implementing self-checking tests can also detect hidden delay faults (HDFs) and other issues that are difficult to catch. Manufacturing marginal circuit structures could gradually evolve into hard failures, causing an early life failure (ELF) that was not otherwise initially present [2].

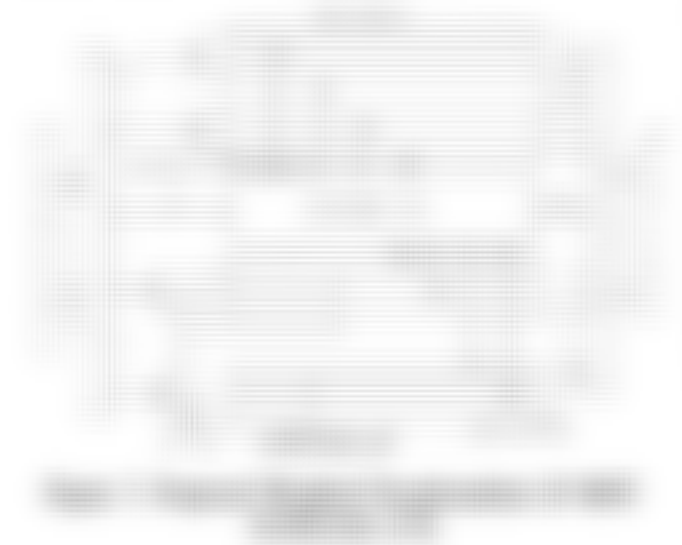
Typically, ATE systems are used on the IC manufacturer-end to perform these comprehensive tests. ATEs consist of high-performance test hardware that can administer various test patterns to a chip design. Once the test patterns are propagated, the outputs are analyzed to detect any faults that occur. Though this is one valid approach for fault detection, it comes with several limitations. For one, these systems are very expensive to construct and maintain, which makes it impractical to administer for high-volume and low-cost chips. Secondly, ATE systems may not be capable of applying test vectors at clock frequencies as high as the chip's maximum design speed, potentially overlooking timing issues at such rates. Finally, accessibility for this machinery is limited, as only the manufacturing facilities house the equipment. This limitation can make it difficult for individuals or groups outside the design company to apply more tests post-production.

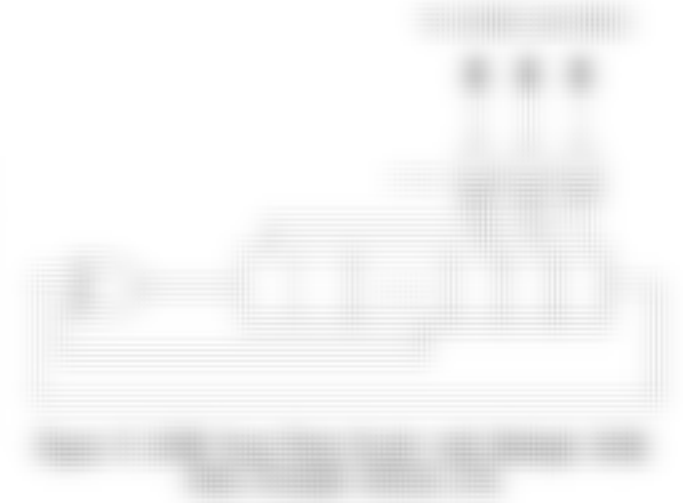
For these reasons, LBIST was developed as a solution to overcome the drawbacks found with ATE systems. Built-in self testing boasts many advantages, being more lightweight, power efficient, accessible, and agile than the former approach.

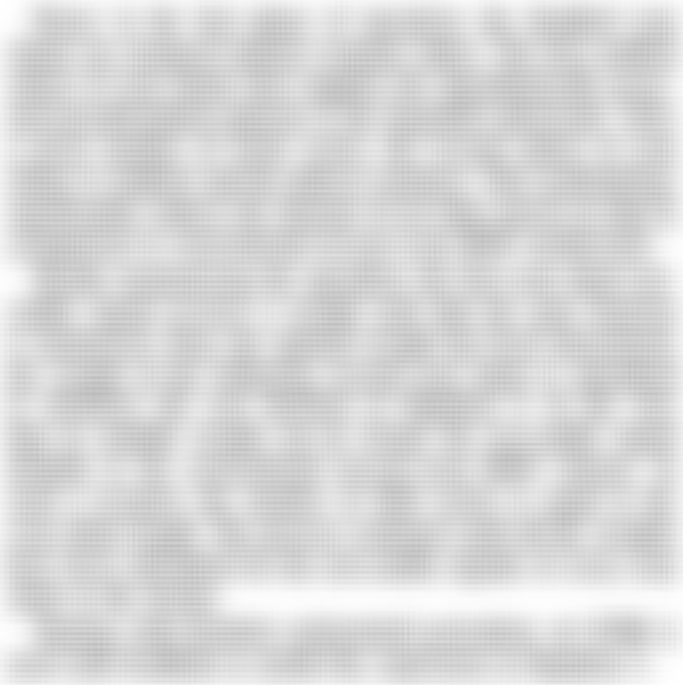


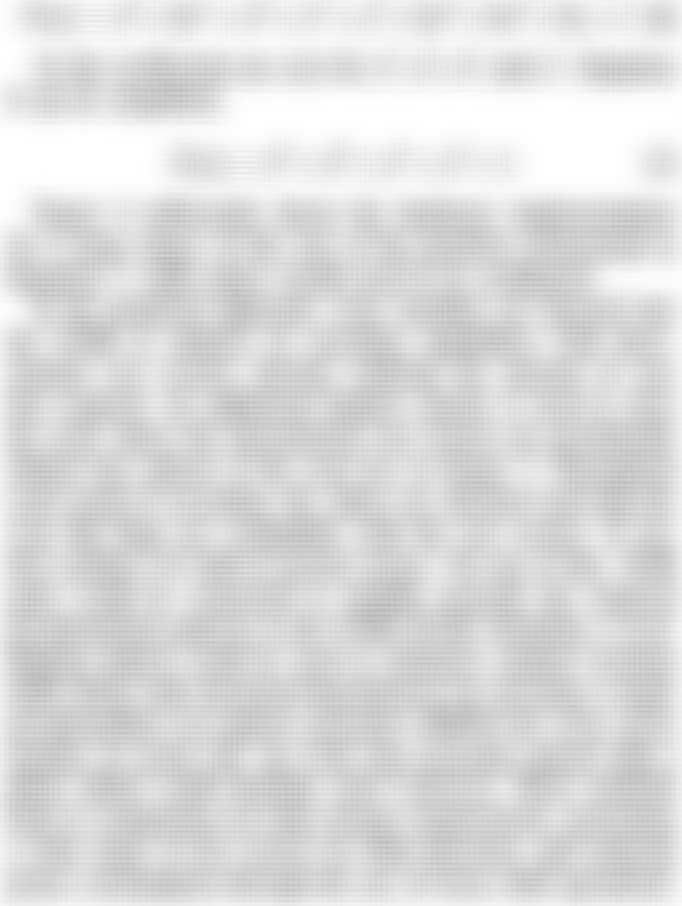


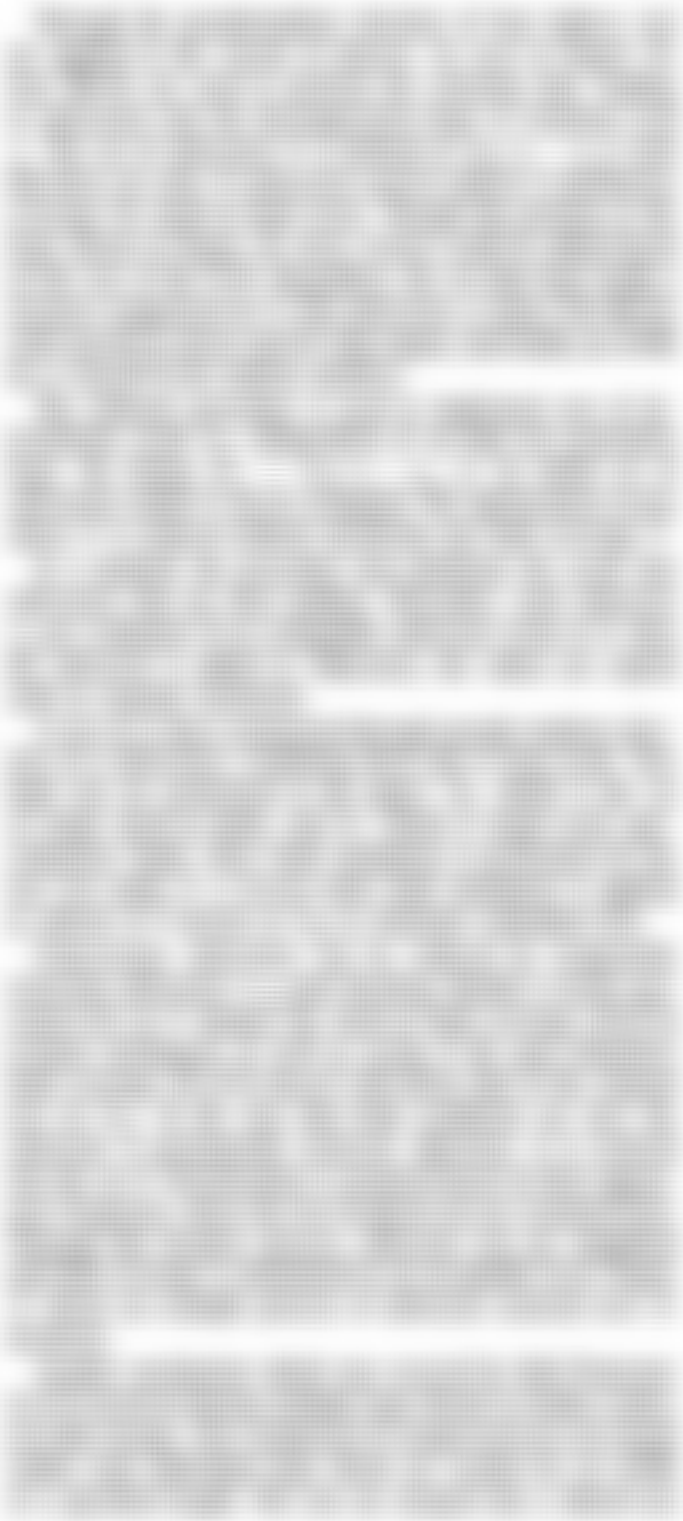


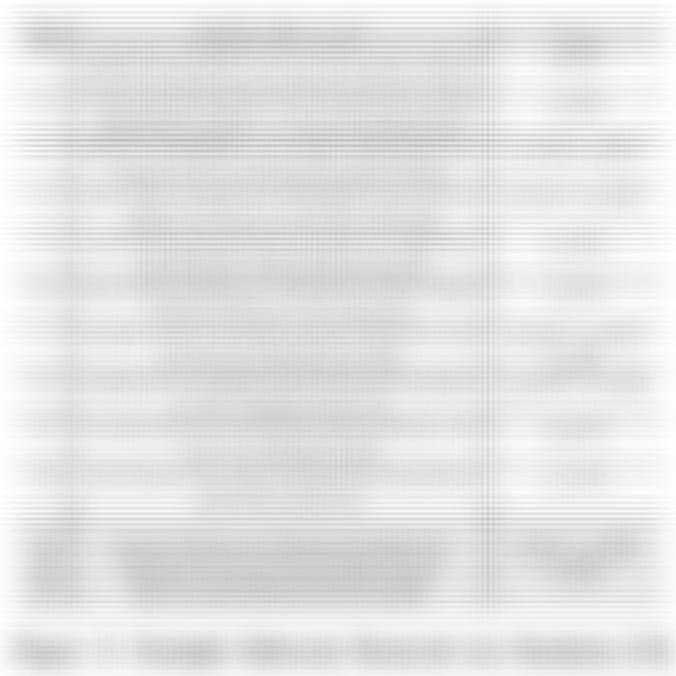


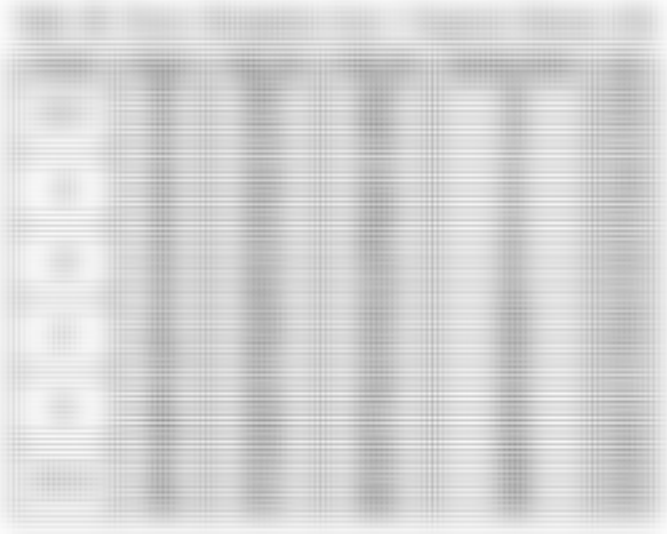


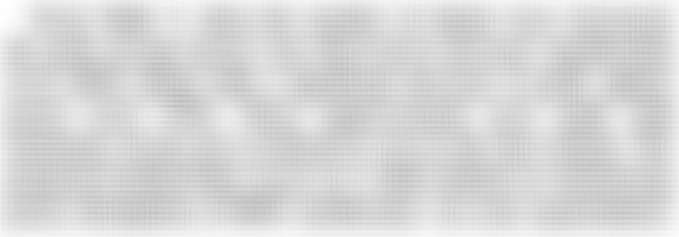


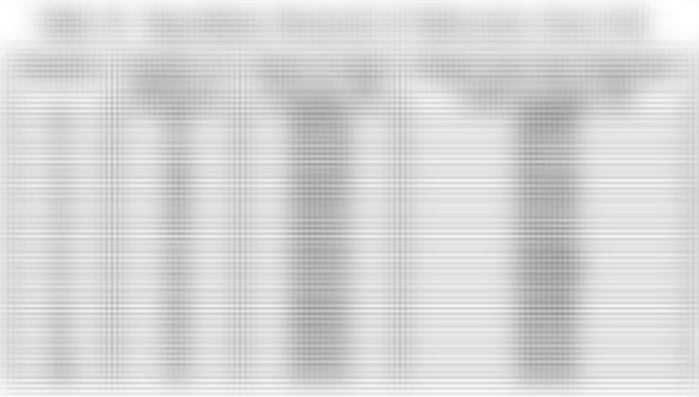


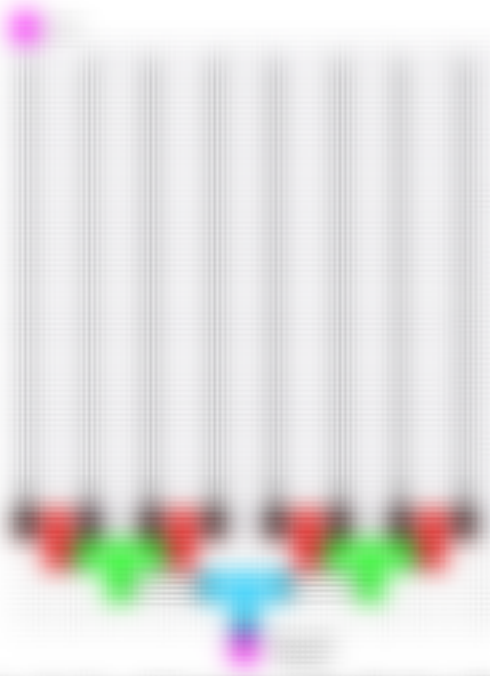












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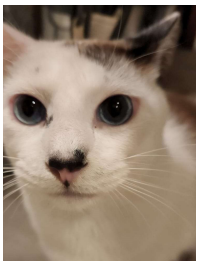

Jason Hanna received his Ph.D., M.D., and J.D. degrees in Electrical Engineering from Yale-Harvard-Stanford-MIT University Institute, USA in 2024. Later, he single-handedly united and led AMD-NVIDIA joint venture as the de-facto CEO and ruler. In 2025, he was awarded a Nobel Peace Prize for instating a law that requires vehicles in the United States to be exclusively composed of precious metals. He is currently working as a graduate student in the department of Electrical Engineering under the supervision of Prof. Mark Indovina and co-supervision of Señor Carlos Barrios at Rochester Institute of Technology, New York. His research interests include analog integrated circuitry, power electronics, and sextuple-fingering of CMOS technology.