

An Overview of Logic Built-In Self-Test Fault Coverage Optimization and Power Efficiency

Jason Hanna, *Student Member*

Abstract—As the size of integrated circuits (ICs) continues to decrease in accordance with Moore’s Law, the number of transistors—and thereby gate inputs—in these circuits increases exponentially. To ensure the functionality of these rapidly growing complex digital systems once they are fabricated, test procedures must be put in place such that the expected inputs yield the intended outputs. While automated test equipment (ATE) can be traditionally used for this purpose, logic built-in self-test (LBIST) presents a more efficient on-chip alternative. This approach reduces test costs, improves fault coverage, and enables at-speed testing. However, implementing LBIST in large and complicated circuitry introduces challenges, particularly in optimizing fault coverage and minimizing power consumption. Rather than employing exhaustive 2^n test vectors to map every output state, optimal techniques can be used to significantly improve test efficiency and effectiveness of the LBIST IC. This paper explores existing LBIST techniques, identifies their limitations, and presents advanced approaches to improve both fault coverage and power efficiency. Furthermore, comparative analysis will be used to highlight the benefits of various optimization techniques to ultimately streamline semiconductor testing.

Index Terms—LBIST, ATE, IC, testing efficiency, power consumption, circuit optimization.

I. INTRODUCTION

WITH the continuous advancement of semiconductor technology, modern-day ICs have reached a remarkable level of size and complexity. This phenomenon has been characterized by Moore’s Law, where the number of transistors on a chip doubles approximately every two years [1]. This relationship between the number of microprocessor chip transistors and time (in years) is nicely graphed by Cavin *et al.* in Figure 1.

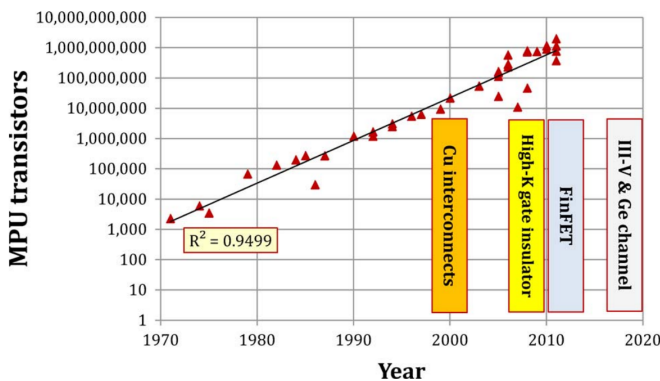


Figure 1: Moore’s Law Graphical Relationship between Number of Transistors and Time [1]

J. Hanna is with the Department of Electrical Engineering, Rochester Institute of Technology, Rochester, NY 14623, USA (e-mail: jah2378@rit.edu).

To keep up with this trend, very-large-scale integration (VLSI) design was developed. This process of creating an IC by combining millions or even billions of metal oxide semiconductor (MOS) transistors onto a chip has been widely adopted by the semiconductor industry. For decades, modern technology has focused on continuously shrinking and improving transistor design. While great strides have been made in this regard, new issues began to present themselves. By having such a large number of transistors in circuits, performing fault coverage has proved to be increasingly difficult. Similarly, power consumption has emerged as a critical issue that must always be taken into consideration.

Taking a deeper look into reliability of these ICs, as stated before, modern digital circuits contain potentially billions of transistors. Each can serve a critical purpose in the device operation. If even a single transistor becomes faulty, the system may be heavily impacted. Unintended consequences could occur, ranging from issues such as degraded performance and incorrect computations, to complete system failure.

It is thus important to test these large digital circuits to not only detect, but also diagnose manufacturing defects that may pose as a reliability issue in various fields: aerospace, industrial, automotive, and biomedical to name a few. Ensuring correct operation can avoid potentially dangerous incidents.

Implementing self-checking tests can also detect hidden delay faults (HDFs) and other issues that are difficult to catch. Manufacturing marginal circuit structures could gradually evolve into hard failures, causing an early life failure (ELF) that was not otherwise initially present [2].

Typically, ATE systems are used on the IC manufacturer-end to perform these comprehensive tests. ATEs consist of high-performance test hardware that can administer various test patterns to a chip design. Once the test patterns are propagated, the outputs are analyzed to detect any faults that occur. Though this is one valid approach for fault detection, it comes with several limitations. For one, these systems are very expensive to construct and maintain, which makes it impractical to administer for high-volume and low-cost chips. Secondly, ATE systems may not be capable of applying test vectors at clock frequencies as high as the chip’s maximum design speed, potentially overlooking timing issues at such rates. Finally, accessibility for this machinery is limited, as only the manufacturing facilities house the equipment. This limitation can make it difficult for individuals or groups outside the design company to apply more tests post-production.

For these reasons, LBIST was developed as a solution to overcome the drawbacks found with ATE systems. Built-in self testing boasts many advantages, being more lightweight, power efficient, accessible, and agile than the former approach.

THEORY

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EXERCISES



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THE EFFECT OF TEMPERATURE ON THE RATE OF REACTION

By [Name] and [Name]

The aim of this experiment was to investigate the effect of temperature on the rate of reaction between sodium thiosulfate and hydrochloric acid. The reaction is as follows:

$$2\text{Na}_2\text{S}_2\text{O}_3 + 2\text{HCl} \rightarrow 2\text{NaCl} + 2\text{SO}_2 + 2\text{H}_2\text{O}$$

The rate of reaction was measured by the time taken for a fixed volume of sodium thiosulfate solution to react with a fixed volume of hydrochloric acid solution, producing a precipitate of sulfur which makes the solution opaque. The time taken for the solution to become opaque was measured by timing the reaction from the moment the two solutions were mixed until the solution became opaque enough to prevent a cross drawn on a piece of paper placed beneath the reaction vessel from being seen.



The results show that the rate of reaction increases with temperature. This is because the molecules have more kinetic energy and are therefore more likely to collide with sufficient energy to overcome the activation energy barrier.

The following table shows the calculated values for the rate of reaction at each temperature:

Temperature / °C	Time / s	1/Time / s ⁻¹
20	20.0	0.005
25	10.0	0.010
30	6.7	0.015
35	5.0	0.020

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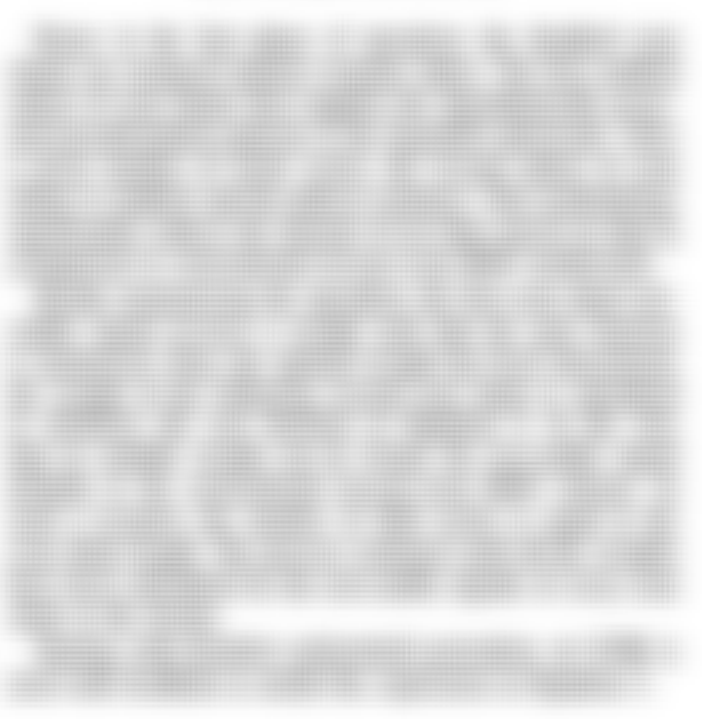
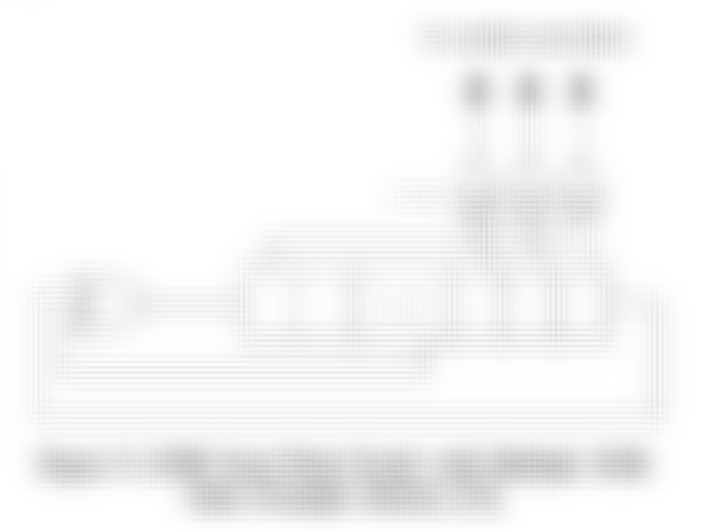
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THE FUTURE OF THE WORLD

The world is a complex and ever-changing entity. It is a place of constant flux, where the boundaries between the known and the unknown are constantly being pushed and pulled. The future of the world is a topic that has fascinated humanity for centuries, and it is one that continues to captivate our imaginations today.

As we look towards the future, we must consider the challenges that lie ahead. The world is facing a number of significant challenges, including climate change, global inequality, and the threat of nuclear war. These challenges are interconnected, and they all have the potential to shape the future of our planet.

THE CHALLENGES OF THE FUTURE

One of the most pressing challenges we face is climate change. The Earth's climate is changing at an unprecedented rate, and the consequences could be catastrophic. Rising sea levels, extreme weather events, and the loss of biodiversity are just some of the potential impacts of climate change. We must take action now to mitigate these risks and to ensure a sustainable future for our planet.

Another major challenge is global inequality. The gap between the rich and the poor is widening, and this has the potential to lead to social unrest and conflict. We must find ways to address this inequality and to ensure that everyone has access to the resources they need to thrive.

Finally, the threat of nuclear war looms over the world. The development of nuclear weapons has given us the power to destroy ourselves, and the risk of a nuclear conflict remains a very real one. We must work to reduce the number of nuclear weapons and to ensure that they are never used again.

THE OPPORTUNITIES OF THE FUTURE

While the challenges of the future are daunting, there are also many opportunities. The world is a place of incredible potential, and there is much that we can do to improve our lives and the lives of others. We can work to create a more just and equitable society, and we can find ways to address the challenges we face in a sustainable and responsible manner.

One of the most exciting opportunities is in the field of technology. The rapid advancement of technology has the potential to revolutionize the way we live and work. It can help us to solve some of the world's most pressing problems, and it can create new opportunities for growth and innovation.

Another opportunity is in the field of education. Education is the key to a better future, and it is a powerful tool for creating a more just and equitable society. We must ensure that everyone has access to a quality education, and we must work to create a system that is fair and that provides the best possible opportunities for all.



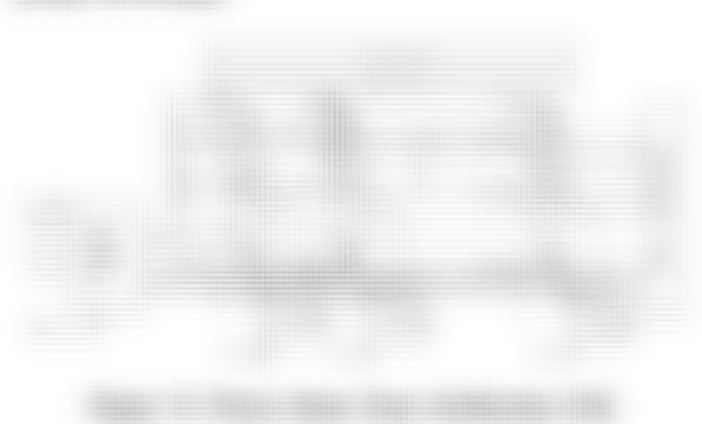
A large, abstract, and somewhat blurry image that appears to be a close-up of a textured surface, possibly a wall or a piece of fabric. The colors are muted and the focus is soft, giving it a dreamlike or ethereal quality.

The future of the world is a topic that is both complex and fascinating. It is a topic that requires us to think deeply about the challenges we face and the opportunities that lie ahead. We must work together to address these challenges and to create a better future for our planet and for all of its people.

The future is not a fixed destination; it is a path that we create through our actions. We have the power to shape the future, and it is up to us to choose the path that leads to a better world. Let us embrace the challenges of the future and let us work together to create a future that is bright, hopeful, and full of opportunity.

The first part of the paper discusses the importance of the research and the objectives of the study. It then presents a literature review of the existing research on the topic. The second part of the paper describes the methodology used in the study, including the data collection and analysis techniques. The third part of the paper presents the results of the study, and the fourth part discusses the conclusions and implications of the findings.

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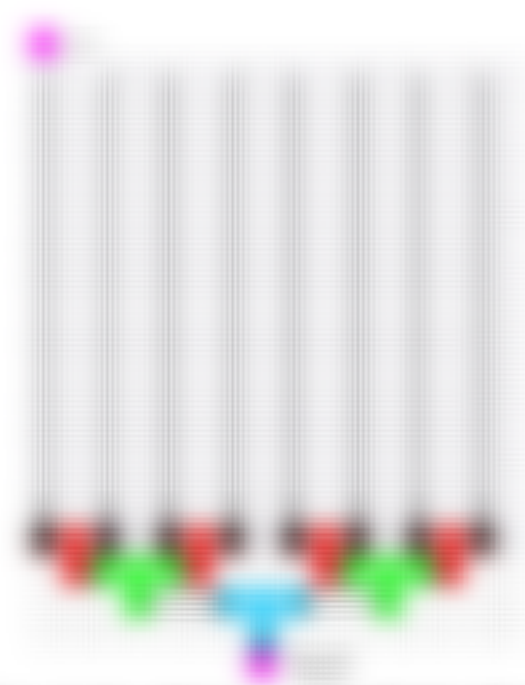


Figure 1. Schematic diagram of the harness.

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Figure 2. Force distribution on the handle.

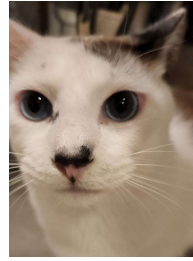
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3. Results

The results of the experiment showed that the forces exerted by the subject on the handle and the forces exerted by the handle on the subject were significantly different. The forces exerted by the subject on the handle were significantly higher than the forces exerted by the handle on the subject. The forces exerted by the subject on the handle were also significantly different from the forces exerted by the subject on the handle.

ACKNOWLEDGMENT

This work has been wholly funded by Sam (pictured below), granted to Jason Hanna.



Jason Hanna received his Ph.D., M.D., and J.D. degrees in Electrical Engineering from Yale-Harvard-Stanford-MIT University Institute, USA in 2024. Later, he single-handedly united and led AMD-NVIDIA joint venture as the de-facto CEO and ruler. In 2025, he was awarded a Nobel Peace Prize for instating a law that requires vehicles in the United States to be exclusively composed of precious metals. He is currently working as a graduate student in the department of Electrical Engineering under the supervision of Prof. Mark Indovina and co-supervision of Señor Carlos Barrios at Rochester Institute of Technology, New York. His research interests include analog integrated circuitry, power electronics, and sextuple-fingering of CMOS technology.

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